WHAT IS CLAIMED IS:

1. A method for manufacturing a contact structure of a wire, comprising steps of:

forming a wire made of aluminum-based material;

depositing an insulating layer covering the wire;

patterning the insulating layer to form a contact hole exposing the wire; and

forming a conductive layer made of indium zinc oxide and electrically connected to the wire.

2. The method of claim 1, wherein the insulating layer is made of nitride silicon.

3. The method of claim 1, wherein the insulating layer is deposited in the range of 280-400 .

4. The method of claim 3, wherein the insulating layer is deposited for a period in the range of 5-40 minute.

5. The method of claim 1, wherein the contact hole is more than 0.5mm X 15μm and less than 2mm X 60μm.

6. The method of claim 1, wherein the contact resistance of the aluminum-based material, and the indium zinc oxide is less than 10% of wire resistance of the wire.

7. The method of claim 6, wherein the contact resistance is less than 0.15 $\mu\Omega cm^2$.

8. A contact structure of a wire, comprising:

a wire of aluminum-based material;

an insulating layer covering the wire and having a contact hole exposing a portion of the wire; and

a conductive layer made of indium zinc oxide on the insulating layer and connected to the wire through the contact hole.

9. The contact structure of claim 8, wherein the contact hole is more than 0.5mm X 15μm and less than 2mm X 60μm.

10. The contact structure of claim 8, wherein the insulating layer is made of nitride silicon.

11. The contact structure of claim 8, wherein the contact resistance of the aluminum-based material, and the indium zinc oxide is less than 10% of wire resistance of the wire.

12. The contact structure of claim 11, wherein the contact resistance is less than 0.15 μΩcm2.

13. A method for manufacturing a thin film transistor array panel, comprising steps of:

forming a gate wire including a gate pad by depositing and patterning an aluminum-based material;

forming a gate insulating layer covering the gate wire;

forming a semiconductor layer;

forming a data wire;

forming a contact hole exposing the gate pad by patterning the gate insulating layer; and

forming a conductive layer electrically connected to the wire by depositing and

patterning indium zinc oxide.

14. The method of claim 13, wherein the gate insulating layer is made of nitride silicon.

15. The method of claim 14, wherein the insulating layer is deposited in the range of 280-400 .

16. The method of claim 13, wherein the indium zinc oxide is formed by sputtering target including In_2O_3 and ZnO.

17. The method of claim 16, wherein the content of Zn in a compound of In_2O_3 and ZnO is in the range of 15-20 at%.

18. The method of claim 13, further comprising the step of:

forming a pixel electrode connected to the data wire when forming the conductive layer.

19. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line, a gate electrode connected to the gate line and a gate pad connected to the gate line, and made of aluminum-based material on an insulating substrate;

depositing a gate insulating layer;

forming a semiconductor layer;

forming a data wire including a data line intersecting the gate line, a source electrode connected to the data line and adjacent to the gate electrode and a drain electrode opposite to the source electrode with respect to the gate electrode by depositing and patterning a conductive layer;

depositing a passivation layer;

patterning the passivation layer along with the gate insulating layer to form a contact hole exposing the gate pad; and

forming a redundant gate pad connected to the gate pad through the contact hole by depositing and patterning IZO.

20. The method of claim 19, further comprising the step of:

forming a pixel electrode connected to the drain electrode when forming the redundant gate pad.

21. The method of claim 19, wherein the data wire further comprises a data pad connected to the data line,

a redundant data pad connected to the data pad when forming the redundant gate pad.

22. The method of claim 19, wherein the insulating layer and the passivation layer are deposited in a temperature range of 280-400 .

23. The method of claim 19, wherein the gate insulating layer and the passivation layer are made of nitride silicon.

24. The method of claim 19, wherein the IZO is formed by sputtering target including In_2O_3 and ZnO.

25. The method of claim 24, wherein the content of Zn in a compound of In_2O_3 and ZnO is in the range of 15-20 at%.

26. The method of claim 19, wherein the data wire and the semiconductor layer are together formed by a photolithography process using a photoresist pattern having different thicknesses depending on the positions.

27. The method of claim 26, wherein the photoresist pattern has a first portion having a first thickness, a second portion having a second thickness thicker larger than the first portion, and a third portion having a third thickness thinner than the first thickness.

28. The method of claim 27, wherein a mask used for forming the photoresist pattern has a first, a second, and a third part, a transmittance of the third part is higher than the first part and the second part, a transmittance of the first part is higher than the second part.

29. The method of claim 28, wherein the first portion and the second portion of the photoresist pattern are respectively aligned on portion between the source electrode and the drain electrode, and the data wire.

30. The method of claim 29, wherein the first part of the mask includes a partially transparent layer, or a pattern smaller than the resolution of the exposure used in the exposing step, to regulate the transmittance of the first part.

31. The method of claim 30, wherein the thickness of the first portion is less than the half of the thickness of the second portion.

32. The method of claim 31, further comprising step of:

depositing an ohmic contact layer between the data wire and the semiconductor layer.

33. The method of claim 32, wherein the data wire, the ohmic contact layer, and the semiconductor layer are formed in the same photolithography process.

34. A thin film transistor array panel, comprising:

a gate wire including a gate pad, and made of aluminum-based material on an

insulating substrate;

a gate insulating layer covering the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire including a data line, a source electrode connected to the data line and adjacent to the gate electrode and a drain electrode opposite to the source electrode with respect to the gate electrode, and made of a conductive material on the gate insulating layer;

a passivation layer covering the data wire; and

a redundant gate pad connected to the gate pad through a contact hole of the gate insulating layer and the passivation layer, and made of indium tin oxide.

35. The thin film transistor array panel of claim 34, further comprising a pixel electrode connected to the drain electrode, and made of the same indium tin oxide as the redundant gate pad.

36. The thin film transistor array panel of claim 34, wherein the data wire further comprises a data pad connected to the data line; and

further comprising a redundant data pad connected to the drain electrode, and made of indium tin oxide with the same layer as the redundant gate pad.

37. The thin film transistor array panel of claim 34, wherein the gate insulating layer and the passivation layer are nitride silicon.

38. The thin film transistor array panel of claim 34, wherein the redundant gate pad is formed on the passivation layer.

39. The thin film transistor array panel of claim 34, wherein the contact resistance of the aluminum-based material, and the indium tin oxide is less than 10% of

wire resistance of the gate wire.

40. The thin film transistor array panel of claim 39, wherein the contact resistance is less than 0.15 Ω °cm^2.

41. The contact structure of claim 34, wherein the contact hole is more than 0.5mm X 15μm and less than 2mm X 60μm.